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Specification

1. Title of the Invention

MOS TYPE INTEGRATED CIRCUIT DEVICE ON INSULATING SUBSTRATE

2. Scope of Claim for a Patent

(1) A MOS type integrated circuit device formed on an insulating substrate in which respective MOS FETs are integrally formed on a plurality of first conductivity type island-like semiconductor regions which are formed on an insulating substrate, characterized in that a first MOS FET including a source area and a drain area of a second conductivity type formed in said semiconductor regions, a conductor layer which is formed under a channel region between said source area and said drain area, and a gate electrode which is formed on said channel region through an insulating film, and a second MOS FET including a source region and a drain region of the second conductivity type formed in said semiconductor regions which is different from said semiconductor region in which said first MOS FET is formed, and a gate electrode which is formed on a channel region between said source and drain regions through an insulating film are selectively employed to configure the circuit.

(2) A MOS type integrated circuit device on an insulating substrate according to claim 1, characterized in that at least a part of said conductive layer of said first MOS FET is electrically connected to said channel region.

(3) A MOS type integrated circuit device on an insulating substrate according to claim 1, characterized in that said conductive layer of said first MOS FET is separated from said channel region through an insulating layer.

3. Detailed Description of the Invention

[Technical Field of the Invention]

The present invention relates to a MOS type integrated circuit device on an insulating substrate in which MOS FETs are integrally formed in island-like semiconductor regions which are formed on an insulating substrate.

[Technical Background of the Invention and its Problems]

In general, in a MOS type integrated circuit device of this sort, since a channel region of a MOS FET is in an electrically floated state, there are disadvantages in that the operation becomes unstable and the back-channel is formed due to the substrate floating effect to increase a drain leakage current.

As the MOS FET which is capable of removing the above-mentioned disadvantages, the device as shown in Figs. 4 and 5 has been proposed in Japanese Patent Application Laid Open No. 59-81278 entitled "MOS TYPE FIELD EFFECT TRANSISTOR ON INSULATING SUBSTRATE" by the present applicant. The MOS FET proposed therein is designed in such a way that a conductor layer 20 is provided under a channel region 25 through an insulating film (a silicon oxide film) 21, and the above channel region 25 and the conductor layer 20 are electrically connected to each other, whereby the carriers which become the cause of the substrate floating effect are caused to flow out through the above conductor layer 20. In addition, the channel region 25 and the conductor layer 20 are the capacitive coupling, and a negative voltage is applied to the above conductor layer 20, whereby the back-channel is prevented from being formed to reduce the drain leakage current. Reference numeral 18 designates a silicon substrate, 19 designates a silicon oxide film, 22 designates a silicon island, 23 designates a source region, 24 designates a drain region, 26 designates a gate insulating film, 27 designates a gate electrode, 28 designates a CVD-SiO_2 and BPSG film, 29a to 29d designate contact holes, and 30 designates an aluminum wiring.

However, when the integrated circuit is constituted by only MOS FETs each having the structure as described above, an area is needed for a part to take out an electrode from the conductor layer 20, which causes reduction of the density of integration. In addition, the degree of integration is also reduced when the wiring is pulled around

from the electrode taking-out part.

[Object of the Invention]

The present invention is accomplished in view of the above matter, and it is therefore an object of the present invention to provide a MOS type integrated circuit device on an insulating substrate in which the reduction of the density of integration can be suppressed, and also the formation of the back-channel which becomes the cause of the kink phenomenon in the static characteristics and the drain leakage current due to the substrate floating effect can be excluded so that superior characteristics can be acquired.

[Summary of the Invention]

That is, in the present invention, in order to attain the above-mentioned object, a conductor layer is provided under a channel region selectively only for a MOS FET constituting a circuit which is sensitive to and has a large adverse effect on such a substrate floating effect and back-channel currents, such as an input buffer circuit or an output buffer circuit. As a result, the reduction of the density of integration is suppressed to a minimum, and also superior characteristics are acquired.

[Embodiments of the Invention]

One embodiment of the present invention will hereinafter be described with reference to the drawings. If it is assumed that in a CMOS type integrated circuit device, an input buffer circuit or an output buffer circuit is constituted by a CMOS inverter, when establishing an interface with the outside, an input voltage V_{IL} with which the level of an output of the CMOS inverter is inverted from a level "H" to a level "L" needs to be made high to some degree. However, if the CMOS integrated circuit device is used under a state in which the channel region of an n-channel MOS FET is floated, the above-mentioned V_{IL} is decreased as compared with the case where the electric potential of the channel region is set to the same as that of the source electric potential (this is represented by a solid line in Fig. 2). Therefore, if the MOS FET having the structure shown in Fig. 4 or Fig. 5 is employed only for the MOS FET constituting a circuit which is sensitive to and has a large adverse effect exerted on such a substrate floating effect and back-channel currents, and also the electric potential of the conductor layer 20 is set equal to the source electric potential (or a

negative voltage is applied thereto), then the voltage V_{IL} is increased as shown by a broken line in Fig. 2 so that superior circuit characteristics are acquired while suppressing the reduction of the density of integration to a minimum. In addition, in the state where the channel region is floated, the back-channel is formed in the n-channel MOS FET and the drain-leakage current is caused to flow, lowering the level "H" of the output voltage V_{out}. However, the lowering of the level "H" of the output voltage V_{out} can also be prevented.

Next, the description will hereinbelow be given with respect to the process of manufacturing the integrated circuit device according to the present invention. Figs. 1(a) to (e) are respectively cross sectional views showing the manufacturing process when forming an n-channel MOS FET on a silicon oxide film (SiO_2). First of all, as shown in Fig. 1(a), a (100) oriented silicon substrate 18 is thermally oxidized to form an oxide film 19 with 5000Å thickness. Then, an amorphous silicon film or a polycrystalline silicon film 20 having a thickness of 3000Å are deposited on the oxide film 19 by utilizing the CVD method. Then, the silicon film 20 thus deposited is changed to monocrystal by utilizing the laser annealing method. At this time, the orientation of monocrystal becomes (100). In this connection, as a means for monocrystallization, in addition to the laser annealing method, the electron beam annealing method, the strip heater method or the like may also be utilized. Next, boron ions are implanted into the monocrystalline silicon 20 at 50 keV with a dose of 2×10^{15} /cm^2 by utilizing the ion implantation method, and then annealing at a high temperature (at 1000°C) is performed for 20 minutes in nitrogen atmosphere to reduce the layer resistance down to 50 Ω/□.

Next, as shown in Fig. 1(b), after the above-mentioned monocrystalline silicon layer 20 was patterned by the photolithography, SiO_2 is deposited thereon by the CVD method. Next, as shown in Fig. 1(c), an opening is selectively formed through a part of the above SiO_2 layer (silicon oxide film) 21 on the area to form a channel region by utilizing the RIE method. Then, a polycrystalline silicon layer with 5000 Å thickness is deposited by utilizing the CVD method and then this polycrystalline silicon layer is changed into monocrystal by utilizing the laser annealing method. The orientation of the monocrystalline silicon layer at this time is (100). The monocrystalline silicon

layer is selectively etched away using the etchant of KOH to form island-like silicon regions (silicon islands) 22a and 22b as shown in Fig. 1(d). Then, in a similar manner to that of the prior art, source regions 23a, 23b and drain region 24a, 24b are respectively formed in the silicon islands 22a and 22b, and gate electrodes 27a and 27b are respectively formed on channel regions 25a and 25b which are respectively formed between the source and drain regions 23a and 24a, and between the source and drain regions 23b and 24b through gate insulating films 26a and 26b to form the gate electrodes 27a and 27b and then to form two kinds of MOS FETs Q1 and Q2 at the same time.

Next, as shown in Fig. 1(e), a CVD-SiO_2 film 28A and a BPSG film 28B are deposited to have a thickness of 8000 Å in total, and the contact holes 29a to 29g are formed therethrough and then an aluminum wiring 30 is formed, thereby taking out the respective electrodes.

Also, in the above-mentioned embodiment, boron ions are implanted into the monocrystalline silicon layer 20 in the process shown in Fig. 1(a), it is to be understood that aluminum ions or the like may also be employed as long as they are p type impurity ions. Then, in the case where a p-channel MOS FET is formed, n type impurity ions such as phosphorous ions, arsenic ions or antimony ions may be employed. In addition, the diffusion method may also be employed for the introduction of the impurity ions into the monocrystalline silicon layer 20.

Fig. 3 is a cross sectional view showing the structure of another embodiment of the present invention. In the above-mentioned embodiment, the hole is formed through the CVD-SiO_2 film 21 to connect the channel region 26a and the conductor layer 20 to each other, whereas in the present embodiment, the silicon island 22a is formed via the CVD-SiO_2 film 21. In Fig. 3, the same constituent parts as those of Fig. 1 are designated by the same reference numerals and the description thereof is omitted here. In this structure as well, substantially the same effects as those in the above-mentioned embodiment can be obtained. In this case, in the process shown in Fig. 1(a), it is not necessary to change the polycrystalline silicon layer 20 into monocrystal by utilizing the laser annealing method.

Also, in each of the above-mentioned embodiments, the description has been given

with respect to the specific case where the MOS FET is formed on the SiO_2 film, it is to be understood that instead of SiO_2 film, other insulating substrates such as SiN, sapphire, MgO and a substrate having a spinel structure may also be employed. In addition, as for the conductor layer which is formed under the channel region of the MOS FET, not only a polycrystalline silicon layer or an amorphous silicon but also high melting point metal such as Mo, Ti, Ta, W and silicide thereof may be employed. In this case, the introduction of the impurity ions into the conductor layer becomes unnecessary.

[Effects of the Invention]

As set forth hereinabove, according to the present invention, it is possible to provide a MOS type integrated circuit device on an insulating substrate in which the decrease of the density of integration can be reduced, and the formation of a back-channel which becomes the cause of the kink phenomenon in the static characteristics and the drain leakage current due to the substrate floating effect can be excluded so that the superior characteristics can be acquired.

4. Brief Description of Drawings

Figs. 1 are cross sectional views useful in explaining the process of manufacturing a MOS type integrated circuit device on an insulating substrate according to an embodiment of the present invention; Fig. 2 is a graphical representation useful in explaining the input and output characteristics of a CMOS inverter; Fig. 3 is a cross sectional view useful in explaining the process of manufacturing a MOS type integrated circuit device on an insulating substrate according to another embodiment of the present invention; and Figs. 4 and 5 are respectively cross sectional views useful in explaining a conventional MOS type integrated circuit device on an insulating substrate.

19: silicon oxide film (insulating substrate), 20: conductor layer, 21: silicon oxide film (insulating film), 22: silicon island, 23: source region, 24: drain region, 25: channel region, 26: gate insulating film, 27: gate electrode.

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